AMENDMENTS TO THE SPECIFICATION

Please amend the Specification as follows:

[0022] In addition, MSP 200 includes an internal memory for local data and variable storage to alleviate bandwidth bottlenecks on the off chip memory. For example, MSP 200 may include a machine readable storage medium such as data random access memory (RAM) 270, as well as a memory command handler (MCH) to handle a plurality of data streams. As illustrated, input PE 220-1, as well as output PE 220-5 handle input and output processing of data streams, whereas PEs 220–2 to 220-4 perform some sort of algorithmic functionality with the use of hardware accelerators 250 (250-1, . . ., 250-n). In addition, each PE 220 may include, for example, 16 local registers and indirect registers which may be, for example, 16 bits wide and can be used for either 16 bit operands or 8 bit operands. In order to perform the desired media processing functionalities, the various PEs utilize register file 210.

[0033] In one embodiment, media processor 400 may be incorporated into a data driven architecture to provide desired media processing functionality. In one embodiment, a data driven media architecture 500 is illustrated with reference to FIG. 11. As such, FIG. 11 illustrates a system level diagram of a data driven media architecture 500 in accordance with one embodiment of the invention. The media architecture 500 includes media processor 400 coupled to machine readable storage mediums such as memory 450 and 440. In one embodiment, the memory is, for example, dual data rate (DDR) synchronous data random access memory (SDRAM) which runs at, for example, 133 MHz (266-MHz DDR devices).